REMARKS

Claims 1-16 and 26-31 are pending after entry of this preliminary amendment. Claims 17-25 have been canceled.

The Specification is herein amended to correct typographical errors and minor omissions in order to more clearly and accurately describe the claimed invention. No new matter has been introduced.

Claims 1 and 10 are herein amended to clarify the present invention, and no new matter is introduced.

New claims 26-31 are submitted, and no new matter is introduced with new claims 26-31.

This preliminary amendment is filed with a continuation of Application Number 09/346,156, filed on June 30, 1999. This continuation is being filed under 37 C.F.R. §1.53(b).

Claims 1 and 10 have been previously rejected in the parent application under 35 U.S.C. § 102(e), as being anticipated by Jain (U.S. Pat. No. 5,821,168), and the Applicant submits the following remarks in reference to Jain.

The present application claims a method for making dual damascene dielectric structures in which a barrier layer is formed over a substrate in which metallization lines have been fabricated. As is known, and as used herein and illustrated in Applicants'

Figures, the term substrate is generally any dielectric layer of a multi-layer semiconductor structure. Metallization lines are formed by etching trenches in the dielectric layer, and then filling those trenches with a desired metal. In the present invention, a barrier layer is then formed over the substrate containing the metallization lines. An inorganic dielectric layer that will define the via layer is formed over the barrier layer. The inorganic dielectric via layer is such that it is highly selective relative to the barrier layer when etched. A low dielectric constant layer that will define the trench layer is then formed over the inorganic dielectric via layer. The low dielectric constant trench layer is of different material properties than the inorganic dielectric via layer, and two distinct etch chemistries are used in forming first the trench structures in the low dielectric constant trench layer, and then the via structures in the inorganic dielectric via layer, in one embodiment of the present invention. Once the trench structures have been etched, the second etch chemistry used to etch the via structures in the inorganic dielectric via layer. The second etch chemistry is optimized to etch through inorganic oxide materials while providing high selectivity to the barrier layer (see the Specification, page 12, lines 9-21).

The inorganic dielectric via layer provides the ability to define the via structures and leave the barrier layer intact until the fabrication process arrives at the process of fabricating the vias. In fact, the barrier layer may not be removed until after an ashing operation is performed to remove the photoresist. The walls of the trench regions and the via holes are then coated with a barrier layer which is preferably a tantalum nitride material or a tantalum material (Specification, page 13, lines 9-13). The ability to leave the barrier intact reduces oxidation of the metallization lines, allows for the barrier layer thickness to be decreased, and thereby reduces overall inter-layer capacitance.

The Applicants therefore are claiming a method in which a low dielectric constant trench layer is formed over an inorganic dielectric via layer which is formed over a barrier layer. It should be noted, as described in Applicants' specification at page 12, lines 6-8, not trench barrier (*e.g.*, a barrier layer between the low dielectric constant trench layer and the inorganic dielectric via layer) is used in the structure of the present invention, thereby further decreasing the dielectric constant of the low dielectric constant trench layer.

Jain does not teach or suggest the claimed invention. Jain teaches a process for forming a semiconductor device which contains two low dielectric constant layers. Jain does not teach a low dielectric constant trench layer over an inorganic dielectric via layer. Jain teaches a first low dielectric constant layer formed over a barrier layer (Col. 3, lines 7-8, Figure 3), and a second low dielectric constant layer formed over an optional etch stop film over the first low dielectric constant layer (Col. 3, lines 13-24, Figure 3).

Applicants respectfully submit that because Jain does not teach a low dielectric constant layer over an inorganic dielectric layer, Jain does not teach or suggest the claimed invention. Additionally, Jain's teaching is contrary to the Applicants' claimed invention in that Jain teaches the optional etch stop (*e.g.*, a trench barrier) between the first and the second low dielectric constant layers. The process taught by Jain is distinct from the present invention, and therefore neither teaches nor suggests the claimed invention.

Applicants submit that all of the pending claims are in a condition for allowance, and a notice of allowance is respectfully requested. If the Examiner has any questions concerning the present preliminary amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in

connection with this filing, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P106A). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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